## REMARKS

Claims 1-4, 7-10, 13-17 and 20-42 were pending in the application.

Claims 1-4, 7-10, 13-17, 20 and 21 have been rejected.

Claims 22-42 have been withdrawn as being directed to a non-elected species and are hereby cancelled without prejudice.

Claims 1-2, 7, 13 and 16 have been amended as shown above.

Claims 43-47 have been added.

Claims 1-4, 7-10, 13-17, 20-21 and 43-47 are now pending in this application.

Reconsideration of the claims is respectfully requested.

## I. CLAIM REJECTIONS – 35 U.S.C. § 102

Claims 1-2, 4, 7-8, 10, 13-17 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,108,945 to Matthews ("*Matthews*"). Claims 1-3, 7, 9, 13 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,091,760 to Maeda et al. ("*Maeda*").

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal*

*Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 U.S.P.Q.2d 1051 (Fed. Cir. 1987)).

**The *Matthews* Reference**

Claim 1 is not taught or suggested by the *Matthews* reference. The *Matthews* reference does not disclose a semiconductor apparatus that includes at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, where an emitter of the double poly bipolar transistor contains a second dopant having a second dopant concentration and a source/drain of the double poly MOS transistor contains the second dopant having the second dopant concentration.

The *Matthews* reference discloses that a boron ion implantation is performed to dope a polysilicon MOS source 68, a polysilicon MOS drain 69, a polysilicon MOS gate 33, and a polysilicon base member 35 of BJT 20. (*Matthews*, Column 14, Lines 40-50). This p+ implant is shown in Figures 14A and 14B by arrows 42. Following the p+ implant, an arsenic ion implantation is performed to dope the emitter 67. (*Matthews*, Column 14, Lines 51-55). The emitter implant is shown in Figures 14A and 14B by arrows 43.

Because of this, in the *Matthews* reference, the emitter 67 of the double poly bipolar transistor is formed after the source 68 and the drain 69 of the double poly MOS transistor has been formed. Also, in the *Matthews* reference, the emitter 67 of the double poly bipolar transistor is formed with a dopant (Arsenic) that is different than the dopant (Boron) of the source 68 and the drain 69 of the double poly MOS transistor. As a result, the *Matthews* reference does not anticipate

or suggest the Applicants' invention as set forth in Claim 1 (and its dependent claims).

For these reasons, Claims 1-2, 4, 7-8, 10, 13-17 and 20 are patentable over the *Matthews* reference.

**The *Maeda* Reference**

Claim 1 is not taught or suggested by the *Maeda* reference. The *Maeda* reference does not disclose a semiconductor apparatus that includes at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, where a base of the double poly bipolar transistor contains a first dopant having a first dopant concentration and a gate of the double poly MOS transistor contains the first dopant having the first dopant concentration.

The *Maeda* reference discloses that the gate of a double poly metal oxide semiconductor is formed from a second polysilicon layer 55 by implanting either an n-type impurity (for NMOS transistors) or a p-type impurity (for PMOS) transistors. The ion implanted impurities have a concentration of $5x10^{15}/cm^2$. (*Maeda*, Column 4, Lines 37-53). A silicide layer 56 may also be deposited over the surface of the semiconductor structure. A silicon dioxide film 30 is then deposited over the surface of the semiconductor structure and patterned to form external base electrode regions 58 and 59 of the PNP and NPN transistors, gate electrode regions 49 and 50 of the PMOS and NMOS transistors, and source/drain electrode regions 61 and 60. (*Maeda*, Column 4, Line 62 to Column 5, Line 2). An oxide film 33 is then formed.

After that, arsenic (As) ions are implanted in a concentration of $5x10^{15}/cm^2$ in the NMOS transistor region to form an n+ source region 28 and an n+ type drain region 29 in self alignment with the gate electrode 50. Also, boron difluorine ($BF_2$) ions are implanted in a concentration of $5x10^{15}/cm^2$ in the PMOS transistor region to form an p+ source region 25 and a p+ type drain region 26 in self alignment with the gate electrode 49. (*Maeda*, Column 5, Lines 12-20).

At the same time, the internal base 34 of the NPN transistor and the internal base 64 of the PNP transistor are formed. Arsenic (As) ions are implanted in a concentration of $3x10^{13}/cm^2$ to form an internal base 64 of the PNP transistor, and boron (B) ions are implanted in a concentration of $3x10^{13}/cm^2$ to form an internal base 34 of the NPN transistor. (*Maeda*, Column 5, Lines 20-26). The source region 28 and the drain region 29 of the NMOS transistor and the source region 25 and the drain region 26 of the PMOS transistor are formed at the same time as the formation of the internal base 64 of the PNP transistor and the internal base 34 of the NPN transistor. The formation of these elements (source region 25, drain region 26, source region 38, drain region 29, internal base 34, internal base 64) occurs after the formation of the PMOS gate 49 and the NMOS gate 50.

The internal base 64 of the PNP transistor and the internal base 34 of the NPN transistor are formed with an ion implant concentration of $3x10^{13}/cm^2$. (*Maeda*, Column 5, Lines 20-26). The PMOS gate 49 and the NMOS gate 50 are formed with an ion implant concentration of $5x10^{15}/cm^2$. (*Maeda*, Column 4, Lines 44-53). Therefore, the base of the double poly bipolar transistor (the internal base 34 of the NPN transistor or the internal base 64 of the PNP transistor)

is formed with a dopant concentration ($3x10^{13}/cm^2$) that is different than the dopant concentration ($5x10^{15}/cm^2$) of the gate of the double poly MOS transistor (the PMOS gate 49 or the NMOS gate 50).

Because of this, in the *Maeda* disclosure, the base of the double poly bipolar transistor is formed after the gate of the double poly MOS transistor has been formed. Also, in the *Maeda* disclosure, the base of the double poly bipolar transistor is formed with a dopant concentration that is different than the dopant concentration of the gate of the double poly MOS transistor.

In addition, the *Maeda* reference does not disclose a semiconductor apparatus that includes at least one double poly bipolar transistor and at least one double poly MOS transistor, where an emitter of the double poly bipolar transistor contains a second dopant having a second dopant concentration and a source/drain of the double poly MOS transistor contains the second dopant having the second dopant concentration.

A third polysilicon layer on the *Maeda* apparatus is used to form an emitter electrode 37 of the PNP transistor, an emitter electrode 40 of the NPN transistor, a source drain electrode 39 of the NMOS transistor, and a source drain electrode 38 of the PMOS transistor. (*Maeda*, Column 5, Lines 34-39). The emitter electrodes 37 and 40 are formed with the source drain electrodes 39 and 38 (and not with the source region 25, drain region 26, source region 28 and drain region 29). That means that the dopant that is applied to the emitter electrodes 37 and 40 is not the same dopant that is applied to the source region 25, drain region 26, source region 28 and drain region 29. The dopant that is applied to the emitter electrodes 37 and 40 has a dopant concentration of $1x10^{16}/cm^2$.

(*Maeda*, Column 5, Lines 43-46). Therefore, the emitter electrode of the double poly bipolar transistor (the emitter electrode 37 of the PNP transistor or the emitter electrode 40 of the NPN transistor) is formed with a dopant concentration ($1x10^{16}/cm^2$) that is different than the dopant concentration ($5x10^{15}/cm^2$) of the source/drain of the double poly MOS transistor (the source region 25, drain region 26, source region 28 and drain region 29).

Because of this, in the *Maeda* disclosure, the emitter of the double poly bipolar transistor is formed after the source/drain of the double poly MOS has been formed. Also, in the *Maeda* disclosure, the emitter of the double poly bipolar transistor is formed with a dopant concentration that is different than the dopant concentration of the source/drain of the double poly MOS transistor.

As a result, the *Maeda* reference does not anticipate or suggest the Applicants' invention as set forth in Claim 1 (and its dependent claims).

For these reasons, Claims 1-3, 7, 9, 13 and 21 are patentable over the *Maeda* reference.

Accordingly, the Applicant respectfully requests that the Examiner withdraw the § 102 anticipation rejections with respect to these claims.

## II. CONCLUSION

For the foregoing reasons, the Applicants respectfully request full allowance of all pending claims and that this patent application be passed to issuance.

The Applicants' attorney has made the amendments and arguments set forth above in order to place this application in condition for allowance. In the alternative, the Applicants'

attorney has made the amendments and arguments to properly frame the issues for appeal. The Applicants make no admission concerning any now moot rejection or objection, and affirmatively deny any position, statement or averment of the Examiner that was not specifically addressed herein.

## SUMMARY

As a result of the foregoing, the Applicants assert that the remaining claims in the patent application are in condition for allowance, and respectfully requests an early allowance of such claims. If any issues arise, or if the Examiner has any suggestions for expediting allowance of this patent application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, LLP

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William A. Munck
Registration No. 39,308

P.O. Drawer 800889
Dallas, Texas 75380
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *wmunck@munckcarter.com*